IN THE CLAIMS

A listing of all claims and their current status in accordance with 37 C.F.R. § 1.121(c) is provided below.

1.-7. (canceled)

8. (currently amended) A stacked die package comprising:

a package substrate having a top side and a bottom side, the top side having a plurality of bond pads ~~provided thereon~~, and the bottom side having a ball-grid array pattern ~~provided thereon~~;

a first semiconductor device mounted on the top side of the package substrate, the first semiconductor device having a plurality of bond pads ~~provided thereon~~;

a silicon interposer mounted on the first semiconductor device, the interposer having a first interposer bond pad and a second interposer bond pad, ~~both lying outside a perimeter of the first semiconductor device,~~ wherein the first and second interposer bond pads are formed by ~~electrically coupled via~~ a conductive trace, and wherein the interposer includes: an interposer substrate; a dielectric layer formed on the interposer substrate; [[a]]the conductive trace formed on the dielectric layer; and a passivation layer formed on the conductive trace, ~~said~~ the passivation layer having a plurality of windows ~~formed therein~~ to expose the conductive trace in areas defining the interposer bond pads; [[and]]

a second semiconductor device mounted on the interposer, the second semiconductor device having a plurality of bond pads ~~provided thereon, wherein at least a portion of said conductive trace lies directly underneath and insulated from said second semiconductor device~~; and

a plurality of bond wires coupled between the bond pads of the package substrate, the first semiconductor device, the silicon interposer, and the second semiconductor device, wherein each of the plurality of bond wires is coupled between two adjacent layers of the stacked die package.

~~a first bond wire connected to one of the plurality of bond pads on said first semiconductor and to the first interposer bond pad;~~

~~a second bond wire connected to the second interposer bond pad and to one of the plurality of bond pads on the semiconductor device; and~~

~~a third bond wire connected to one of the plurality of bond pads on the top side of the package substrate and to a bond pad on the first semiconductor device.~~

9. (currently amended) The stacked die package of claim 8, wherein [[said]] the interposer substrate comprises silicon.

10. (currently amended) The stacked die package of claim 8, wherein [[said]] the package substrate comprises a material selected from the group consisting of ceramic, polyimide, metal, glass-filled resin, and cyanate-glass.

11. (currently amended) The stacked die package of claim 8, wherein [[said]] the package substrate includes multilevel metallization.

12. (currently amended) The stacked die package of claim 8, wherein [[said]] the interposer passivation layer comprises silicon nitride.

13. (canceled)

14. (new) A stacked die package comprising:

a substrate layer having a plurality of bond pads;

a first semiconductor layer having a plurality of bond pads, the first semiconductor layer mounted on the substrate layer;

a silicon interposer layer mounted on the first semiconductor layer, the interposer layer having a first bond pad and a second bond pad formed by a conductive trace extending at least partly within the interposer layer; and

a second semiconductor layer mounted on the silicon interposer layer, the second semiconductor layer having a plurality of bond pads.

15. (new) The stacked die package of claim 14, comprising a plurality of bond wires each coupled between a bond pad of one layer and a bond pad of an adjacent layer.

16. (new) The stacked die package of claim 14, wherein the silicon interposer layer comprises a substrate, a dielectric layer formed on the substrate, the conductive trace formed on the dielectric layer, and a passivation layer formed on the conductive trace, the passivation layer having a plurality of openings configured to expose the conductive trace and to form the first and second bond pads.

17. (new) A die package comprising:

a substrate;

a first semiconductor mounted on the substrate;

a silicon interposer mounted on the first semiconductor device;

a second semiconductor mounted on the silicon interposer wherein the substrate, the first and second semiconductors, and the silicon interposer each comprise a plurality of bond pads; and

a plurality of bond wires each coupled between a bond pad of one layer and a bond pad of an adjacent layer.

18. (new) The die package of claim 17, wherein the silicon interposer comprises a plurality of conductive traces extending through the interposer, each conductive trace configured to form a first and a second bond pad and to electrically couple the first and second bond pads together.

19. (new) The die package of claim 17, wherein the silicon interposer comprises a plurality of conductive traces on the surface of the interposer, each conductive trace configured to electrically couple the first and second bond pads together.